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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/044,549	01/11/2002	James B. Keller	5580-00901	9129

34399 7590 11/15/2004

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EXAMINER	
DU, THUAN N	

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 11/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/044,549	KELLER ET AL.	
	Examiner	Art Unit	
	Thuan N. Du	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 January 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8/22/02*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. It is hereby acknowledged that the following papers have been received and placed of record in the file: Preliminary Amendment (dated 1/11/02), Drawings (dated 3/12/02) and IDS (dated 8/22/02).

2. Claims 1-12 are presented for examination.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kawauchi (U.S. Patent No. 6,519,709).

5. Regarding claim 1, Kawauchi teaches a circuit comprising:

a buffer for storing data, wherein the buffer includes a plurality of entries [Fig. 1, memory 12; col. 7, lines 22-23];

a write pointer coupled to the buffer [Fig. 1, circuit 15], wherein the write pointer is configured to sequentially indicate each one of the plurality of entries in the buffer into which data is to be written, wherein the write pointer is clocked by a first clock (input clock 14) [col. 6, lines 38-48];

a read pointer coupled to the buffer [Fig. 1, circuit 17], wherein the read pointer is configured to sequentially indicate each one of said plurality of entries in the buffer from which data is to be read, wherein the read pointer is clocked by a second clock (output clock 18) [col. 6, line 63 to col. 7, line4]; and

a first circuit configured to generate a pointer value in response to an indication that a predetermined pattern of data is transmitted to the buffer for storage, wherein the first circuit is coupled to the read pointer [Fig. 1, circuit 15; col. 6, lines 48-51];

a circuit coupled to the read pointer and to receive the indication, wherein the circuit is configured to generate a signal to the read pointer responsive to the indication [Fig. 1, circuit 16; col. 6, lines 52-62];

wherein said read pointer is configured to update to the pointer value from the first circuit responsive to the signal [col. 7, lines 35-42].

Kawauchi does not explicitly name the circuit 16 is synchronizing circuit. However, the claimed synchronizing circuit does not perform any synchronization function. Therefore, the circuit 16 of Fig. 1 disclosed by Kawauchi is interpreted as the claimed synchronizing circuit.

6. Regarding claim 2, Kawauchi teaches that the value is a write pointer value of the write pointer with the indication, and wherein the circuit is a storage circuit configured to capture the write pointer value in response to the indication [col. 6, lines 48-51].

7. Regarding claim 3, logic circuit, by definition (Microsoft Bookshelf Basics), is a computer switching circuit that performs problem-solving functions. Kawauchi teaches a system for transferring data between two asynchronous clocked circuits via a buffer (a problem-solving

system). Therefore, one of ordinary skill in the art would have recognized that Kawauchi, inherently, including logic circuit.

8. Regarding claim 4, Kawauchi teaches that the indication is synchronized with the second clock [col. 2, lines 60-65].

9. Regarding claims 5-8, one of ordinary skill in the art would have recognized that it would have been obvious to use delay circuit for synchronizing one signal with another. Flip-flops have been widely uses as delay circuits.

10. Regarding claims 9-12, Kawauchi teaches that the data position is counted [col. 9, line3-4]. Therefore, inherently, Kawauchi includes counter in the system.

11. Regarding claim 13, Kawauchi teaches the detecting of data entries in the buffer [col. 6, lines 40-48].

12. Regarding claims 14-21, since they recite method of operating of the apparatus defined in the apparatus claims, they are rejected accordingly based on the rejection of the apparatus claims.

Conclusion

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thuan N. Du whose telephone number is (571) 272-3673. The examiner can normally be reached on Monday and Wednesday-Friday: 10:00 AM - 8:30 PM, EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne H. Browne can be reached on (571) 272-3670.

Central TC telephone number is (571) 272-2100.

The fax number for the organization is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll free).

Thuan N. Du
November 10, 2004